WHAT IS CLAIMED IS:

1. A scan test circuit incorporated into an integrated circuit, the scan test circuit comprising:

a first flip-flop having a reset input terminal for input of a reset signal, the first flip-flop also receiving a data signal, a scan data signal, and a scan shift enable signal, selecting the data signal or the scan data signal according to the scan shift enable signal, and providing the selected signal as output data; and

a reset control circuit for controlling the reset signal according to the scan shift enable signal.

2. The scan test circuit of claim 1, wherein the reset control circuit controls the reset signal so that the reset signal is enabled only while the scan shift enable signal selects the data signal.

3. The scan test circuit of claim 1, wherein the reset control circuit comprises a logic gate receiving the scan shift enable signal and a reset control signal output from a combinatorial circuit in the integrated circuit.

4. The scan test circuit of claim 3, wherein the reset control circuit inverts the scan shift enable signal and ANDs the inverted scan shift enable signal with the reset control signal.

5. The scan test circuit of claim 4, wherein the combinatorial circuit comprises an AND gate receiving output signals of second and third flip-flops, the second and third flip-flops forming a scan chain together with the first flip-flop.

6. The scan test circuit of claim 1, further comprising:
a mask circuit for masking the reset signal; and
a mask control circuit for controlling the mask circuit.

7. The scan test circuit of claim 6, wherein the mask circuit comprises a logic gate for modifying the scan shift enable signal according to an output signal from the mask control circuit and supplying the modified scan shift enable signal to the reset control circuit.

8. The scan test circuit of claim 6, wherein the logic gate in the mask circuit is an OR gate receiving the scan shift enable signal and the output signal from the mask control circuit.

9. The scan test circuit of claim 6, wherein the mask control circuit comprises a flip-flop into which arbitrary data can be loaded.

10. The scan test circuit of claim 6, wherein the mask control circuit comprises:
an input terminal for input of arbitrary data; and
a signal line for supplying the arbitrary data to the mask circuit.